

REMARKS

Status of the Claims:

The Office Action dated April 7, 2004 has been received and reviewed by the applicant. Claims 1-6 are in the application. Claims 1-5 stand rejected and claim 6 stands objected to. Reconsideration is respectfully requested.

Claim Rejection - 35 USC § 102

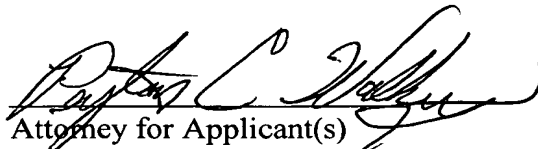
Claims 1, 2, 4 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by US Pat. No. 5,115,458, Burkey et al. In response, a declaration is enclosed herewith for clarifying the technical disclosure of Burkey et al. As disclosed in detail in the declaration, at the second time period as in claim 1, Burkey et al. are silent as to "holes" and consequently do not disclose "holes," but disclose how the "electrons" are transferred. As a reminder, it is pointed out that the "electrons" are the image portion and "holes" are a "by-product" that must be dealt with separately. Therefore, the claimed invention is not taught or suggested by the prior art of record.

Summary

Should the Examiner consider that additional amendments are necessary to place the application in condition for allowance, the favor is requested of a telephone call to the undersigned counsel for the purpose of discussing such amendments.

For the reasons set forth above, it is believed that the application is in condition for allowance. Accordingly, reconsideration and favorable action are respectfully solicited.

Respectfully submitted,


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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

David L. Losee, et al

METHOD FOR REDUCING DARK
CURRENT IN CHARGE COUPLED
DEVICES

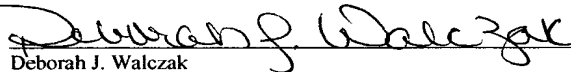
Serial No. 09/660,105

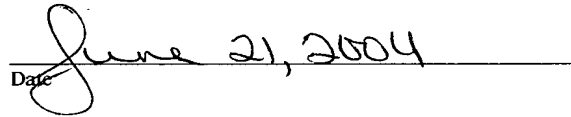
Filed 12 September 2000

Group Art Unit: 2612

Examiner: Hannett, James M.

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today with the United States Postal Service as first class
mail in an envelope addressed to Commissioner For
Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Deborah J. Walczak


Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

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JUN 25 2004

Technology Center 2600

Sir:

DECLARATION UNDER 37 CFR 1.132

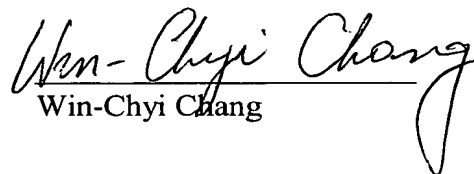
Win-Chyi Chang declares that he is a co-inventor of US Patent 5,115,458 entitled "Reducing Dark Current In Charge Coupled Devices"; that he has reviewed the office action for US Patent Application 09/660,105; that on page 3, the first 6 lines of the office action, where it concludes "holes" are discussed is technically inaccurate; that Burkey et al. (my invention) do not disclose in column 6, lines 1-11 where the holes from the gate connected to $\Phi 1$ go; that US Patent Application 09/660,105 explicitly states that the holes from the second set of gate electrodes are accumulated beneath the first set of gate electrodes by applying a second voltage to the first set of gate electrodes (taking the first set of gate electrodes to an even more negative voltage); that Burkey et al. (my invention) discloses in lines 4-7 the step of performing "the normal clocking sequence to transfer charge from one stage to the next" will cause the holes that were under the gate connected to $\Phi 1$ to be lost to the p-type substrate or p-well; that this loss of holes is depicted in US Patent Application 09/660,105 Figure 2b (Prior Art) time step t1 by the lack of '+' symbols under one gate electrode; that US Patent Application 09/660,105 as depicted in Figure 3b time step t1 shows an extra set of

'+' symbols to indicate the holes under gate $\Phi 1$ are stored under gate $\Phi 2$ by taking gate $\Phi 2$ further into accumulation (a more negative gate voltage); that placing the excess holes underneath the second gate (US Patent Application 09/660,105), instead of pushing the excess holes into the substrate (Burkey et al, my invention), significantly increases the efficiency of charge transfer while maintaining low dark current generation rates which is the advantageous effect of the invention.

He further declares that all statements made herein, of his own knowledge, are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Please charge the fee to Eastman Kodak Company Deposit Account No. 05-0225. A duplicate copy of this request is enclosed.

Respectfully Submitted,


Win-Chyi Chang